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(12) # EUROPEAN PATENT APPLICATION

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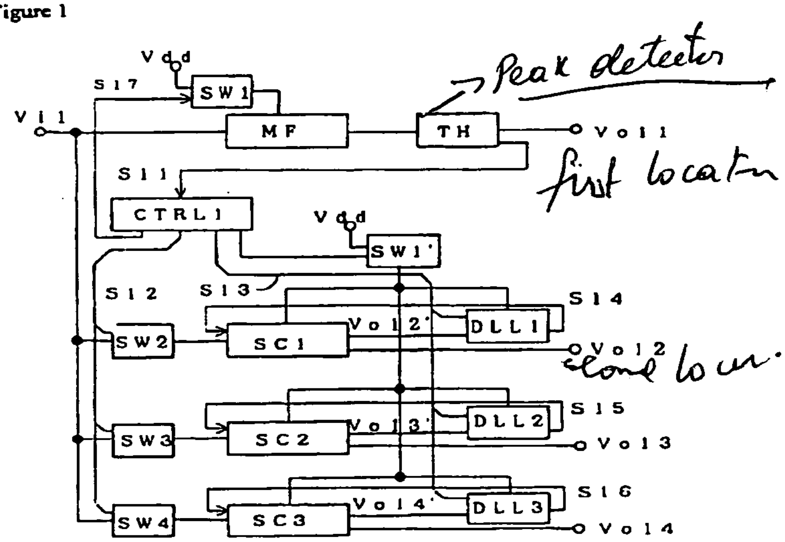
(54) ## Acquisition and tracking filter for spread spectrum signals

(57) The present invention has an object to provide a filter circuit largely reducing electric power to consume compared with a conventional one, as well as realizing the first acquisition in enough high speed. In a filter circuit according to the present invention, a matched filter and a sliding correlator are used in parallel, the first acquisition and holding is executed by a matched filter, a correlating operation is executed by a sliding correlator and a voltage is stopped to supply to the matched filter.

Figure 1



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Description

FIELD OF THE INVENTION

The present invention relates to a filter circuit, especially to a filter circuit effective for a spread spectrum communication system for the mobile cellular ratio and wireless LAN.

BACKGROUND OF THE INVENTION

A matched filter is a filter for judging the identification between two signal. In the spread spectrum communication, each user who receives a signal processes a received signal by a matched filter using spreading code allocated for the user so as to find a correlation peak for acquisition and tracking.

Here, assuming that a spreading code is d(i), sampling interval is Δ t, a length of spreading code is N, a received signal before a time t is x(t-i Δ t), a correlation output y(t) of matched filter is as in formula (1). In formula (1), d(i) is a data string of 1 bit data.

$$y(t) = \sum_{i=0}^{N-1} d(i)x(t - i\Delta t) \qquad (1)$$

Using a matched filter, the size of a circuit was large because a lot of multiplications must be performed. In order to find a aquisition and holding, double sampling or higher order of sampling for acquisition was necessary, but the size of the circuit was larger to execute it. Therefore a matched filter consumed a lot of electric power, which was a defect of it, especially it was a serious defect for the mobile radio communication. A sliding correlator is also known, which sequentially multiply a spread code by a multiplier. It took rather long time to find the first acquisition.

SUMMARY OF THE INVENTION

The present invention solves the conventional problems and has an object to provide a filter circuit largely reducing electric power to consume compared with a conventional one, as well as realizing the first acquisition in enough high speed.

In a filter circuit according to the present invention, a matched filter and a sliding correlator are used in parallel, the first acquisition and holding is executed by a matched filter, a correlating operation is executed by a sliding correlator and a voltage is stopped to supply to the matched filter.

It is possible to control electric power consumption in minimum and the first acquisition is high speed by the filter circuit according to the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a first embodiment of a filter circuit of the present invention.
Figure 2 shows a circuit of a matched filter in the first embodiment.
Figure 3 shows a circuit of a sliding correlator in the first embodiment.
Figure 4 shows a DLL circuit in the first embodiment.
Figure 5 shows a circuit of supply voltage.
Figure 6 shows a circuit of another matched filter.
Figure 7 shows a sampling and holding circuit in the matched filter in Figure 6.
Figure 8 shows a circuit of a multiplexer in the matched filter in Figure 6.
Figure 9 shows the first addition circuit in the matched filter in Figure 6.
Figure 10 shows a circuit of an inverted amplifying portion in the matched filter in Figure 6.
Figure 11 shows a circuit of the second addition circuit in the matched filter in Figure 6.
Figure 12 shows a circuit of the third addition circuit in the matched filter in Figure 6.
Figure 13 shows a circuit of the reference voltage generating circuit in the matched filter in Figure 6.

PREFERRED EMBODIMENT OF THE PRESENT INVENTION

Hereinafter a filter circuit of the present invention is described with referring to the attached drawings.

In Figure 1, the filter circuit includes a matched filter MF connected to an input signal Vi1, and a peak detecting circuit TH is connected to an output of the matched filter MF. A peak detector finds a plurality of timings on which an output of the matched filter exceeds a predetermined level, and outputs a signal showing the timing. The timing of the peak is

a signal of the receiving terminal and timing to receive the delay signal.

An input signal Vi1 is input to the switches of three systems SW2, SW3 and SW4, and through them to sliding correlators of three systems of SC1, SC2 and SC3. DLL (Delay Locked Loop) circuits as time trackers DLL1, DLL2 and DLL3 are connected to the following stages of sliding correlators from SC1 to SC3. The feedback signals (S14, S15 and S16 in Figure 1) are input to sliding correlators.

An output signal S11 of the peak detecting circuit TH is input to a controller CTRL1, and the timings of the sliding correlators from SC1 to SC3 are settled by the controller. The controller conducts and cuts off the switches from SW2 to SW4 by a control signal S12, and basic timings of DLL1 to DLL3 is settled by a control signal S13.

The basic timing settlement means the function to give off-set of d(i+j Δ t) to d(i) in order to adapt the relationship between a spread code d(i) and x(t-i Δ t).

As shown in Figure 2, the matched filter MF includes a plurality of serial sampling and holding circuits S and multipliers (shown by "×" in Figure 2) multiplying from m1 to mn to outputs of the sampling and holding circuits. The sum of outputs of the multipliers is calculated by the adder (shown by "Σ" in Figure 2). Though a matched filter consumes large quantity of electric power because a lot of sampling and holding circuits, multipliers and adders, electric power consumption can be reduced by a power switch controlled by a signal S17 from the controller CTRL1. As shown in Figure 1, the supply voltage VDD of the matched filter is supplied through supply voltage switch SW1 (shown as a representative of a plurality of supply voltage switches).

The sliding correlator and DLL circuit are supplied voltage through supply voltage switch SW1' (shown as a representative of a plurality of supply voltage switches). When the matched filter works for the aquisition at first, the supply voltage switch is opened. The electric power consumption on the first aquisition can be reduced and electric power consumption of the whole circuit is in the minimum.

When the peak is detected in the outputs of the matched filter and signal S11 showing the basic timing is output, the controller CTRL outputs signal S17, so as to open the supply voltage switch SW1. That is, the matched filter is used with respect to the first aquisition and high speed processing is realized than using a sliding correlator, then the matched filter is stopped after the first acquisition is completed. Therefore, electric power consumption after the aquisition is reduced. At the same time that SW1 is conductive, SW1', SW2, SW3 and SW4 are closed and it is started to input signals to SC1 to SC3 and to process signal.

As shown Figure 3, a sliding correlator SC1 once holds input signal Vi3 from a switch SW2 in a sampling and holding circuit S and input it to a multiplication portion (shown by "×"). The multiplication portion multiplies the input signal by a multiplier mi(t) supplied from DLL1, and input it to a low-pass filter LPF as an accumulator. In LPF, one cycle (period of multiplications with all spreading codes) of integration of multiplication results is performed and output the integrated result as output signal Vol2. The multiplier is shown by the function of time, differently from the matched filter, in order to show a subtle settlement of time in DDL1. The input signal (a signal before a multiplication is performed) becomes an input signal Vo12' for DLL1 on the timing of the multiplication after once held. As the structures of sliding correlators SC2and SC3 are the same as that of SC1 above, they are omitted to be described. As the structures from DLL1 to DLL3 are the same, DLL1 is described below and others are omitted.

In Figure 4, DLL1 includes multipliers (shown with "×") which receives parallelly a signal Vo12'. The outputs of them are input to low-pass filters LPF1 and LPF2. The structure of them is the same as the operational part of sliding correlator. They perform a correlation calculation of a signal subtly delayed or gained relative to mi(t). Outputs of LPF1 and LPF2 are input to square-law detectors DET1 and DET2, respectively. The difference of outputs of square detector is calculated by an adder (shown by "+"). The signal of difference is smoothed by a loop filter LF for noise reduction, and input to voltage control oscillation VCO. VCO performs phase control of PNG of spreading code generator in the last step, and generates signals mi(t) for providing SC1, mi(t-Δ) gained by a time Δ than mi(t) and mi(t+Δ) delayed by a time Δ than mit(t). These gained and delayed signals are input to the multiplier and the delay and gain can be always watched.

As above, the size of the circuit of a sliding correlator and a time tracker for sampling and holding and multiplication is smaller, and consuming electricity is less than that of matched filter. The shift of synchronisity can be followed by the time tracker. On starting a new communication, aquisition by a matched filter is started again.

In Figure 1, one switch of supply voltage is shown with respect to whole of a matched filter. The number of supply voltages is to be decided considering the capacity of electricity. For example in Figure 2, one supply voltage should be provided for each sampling and holding circuit and for each multiplication circuit.

Figure 5 shows an example of a supply voltage switch SW1. An input voltage V5 is connected to a drain of a transistor circuit T51 for alternatively connecting a drain and a source of a pair of MOS transistors of n-type and p-type. The source of T51 is connected to an output terminal To5 through a dummy transistor with similar structure with the source T51. S17 is input to a gate of nMOS transistor of the transistor circuit T51, and a signal inverted S17 by an inverter I5 is input to agate of pMOS transistor. When S17 is high level, T51 is conductive, and when it is low level, T51 is unconductive by it. Such a switch itself consumes very low electric power, and has a little influence on whole of electric power consumption.

Here a matched filter with further reduced electricity is described.

In Figure 6 of a matched filter circuit, input voltage Vin is connected in parallel to a plurality of sampling and holding circuits from S/H51 to S/H56. Two types of outputs of H(high) and L(low) are generated from each sampling and holding circuit. A control circuit CTRL is connected to each sampling and holding circuit in order to control that Vin is input to one of the sampling and holding circuits.

According to the control of the control circuit, the sampling and holding circuit inputs an input voltage Vin to either of H or L and a reference voltage Vr to another. The route is selected corresponding to 1 bit sign to be multiplied to an input signal. The multiplication is completed on this step.

Sampling and holding circuits from S/H 51 to S/H56 are structured as in Figure 7 (S/H51 represents them in Figure 7), in which an input voltage Vin is connected to a switch SW6 which is similar to SW1. An output of the switch SW6 is connected to a capacitance C6 whose output is connected with an inverted amplifying portion AMP6.

In Figure 10 of the inverted amplifying portion AMP6, an input voltage V10 is input to three serial stages of MOS inverters I101, I102 and I103. An output Vo10 of the last stage MOS inverter I103 is connected to an input of the first capacitance I101 through a feedback capacitance CF10, consequently, closed loop gain is formed. The capacity of the feedback capacitance CF10 is settled equal to the total capacity of the capacitive coupling connected to the input of CF10 or that of connecting capacitance. The closed loop gain is settled as -1.

In the inverted amplifying portion AMP6, an output of I103 is connected to the ground through a grounded capacitance CG10, and an output of I102 is connected to a voltage supply and ground through a pair of balancing resistance RE101 and RE102. Unstable oscillation of amplifying circuit including feedback line is prevented by it. As a resistance RE101 and inverters from I101 to I103 are connected to the supply voltage through a voltage supply switch SWS structured by well-known analog switch, the electric power consumption is reduced by opening the supply voltage switch when AMP6 does not substantially work.

An output of AMP6 is input to two multiplexers MUX61 and MUX62 to which a common reference voltage Vr is connected. When SW6 is closed, C6 is charged by the electrical charge corresponding Vin, and the linearity of output is guaranteed by the feedback function of AMP6. When the switch SW6 is opened after that, the sampling and holding circuit S/H51 holds Vin.

The switch SW6, multiplexers MUX61 and MUX62 are controlled by control signals S61, S62 and S63. S61 once closes the switch SW6 and then, opens the SW6 on the timing for inputting an input voltage. S62 and S63 are signals reverse to each other. When one of the multiplexers outputs Vin, the other outputs Vr. The MUX61 generates an output of H(high) and the MUX62 generates an output of L(low). The H and L correspond to spreading codes "1" and "-1", respectively. When "1" is multiplied to an input voltage on a time, Vin is output from MUX61, and when "-1" is multiplied, Vin is output from MUX62.

In Figure 8, the multiplexer MUX61 includes transistor circuits T81 and T82 in which a pair of transistors of pMOS and nMOS are connected to each other. An input voltage V8 and the reference voltage Vr are connected to the drains of T81 and T82, respectively. A signal S8 is input to the gate of nMOS and an inverted signal of S8 by an inverter I8 is input to the gate of pMOS of the transistor circuit T81. S8 is input to the gate of pMOS and the inverted signal is input to the gate of nMOS of the transistor circuit T82. The sources of T81 and T82 are connected to a common output terminal To8. When S8 is high, V8 is output from To8, and when it is low, Vr is output from To8 in the multiplexer above.

The signal S62 corresponds to the spreading code. When S62=1, $1 \times$ Vin=Vin is output to AD1p. At the same time, S63 is -1, and an output Vr corresponding to 0 is output to AD1m. When S62=-1, Vr corresponding to 0 is output AD1p. At this time, S63 is +1, and an output $1 \times$ Vin=Vin is output to AD1m. The spreading code is constant for one set of input signals at a timing. On the timing to input a new signal, anew signal is input instead of the oldest signal. At the input, the relationship between circuits 5/H51 to S/H56 and the data d(i) is shifted, therefore, control circuit shifts d(i) relative to the sampling and holding circuits. If the code sequence for S/H51 to S/H56 is not shifted, a signal (data) between (S/H)s is transmitted and an error is caused on the transmission. That is, it is effective to shift a code to prevent an error at data transmission.

The accumulation in the formula (1) is executed by the addition portions AD1p, AD1m, AD52 and AD53, in which output voltage VH and VL of each sampling and holding circuit are accumulated in AD53 and AD52, respectively. These accumulations are not directly executed. Dividing the circuits from S/H51 to S/H56 into a plurality of groups, the outputs VH and VL are once accumulated in AD1p and AD1m in each group. All the outputs of AD1p for accumulating VH are input to AD52, and all the outputs of AD1m for accumulating VL are input to AD53. In Figure 6, six (S/H)s from 51 to 56 are shown, which are divided into three groups,. Generally a spreading code is a hundred or more bits, and sampling and holding circuits are provided by the number corresponding to the number of bits.

As shown in Figure 9, addition portion AD1p (AD1m is the same) includes a capacitive coupling CP9 with capacitances C91, C92 and C93 of a number corresponding to the number of sampling and holding circuit. A normalized addition is performed in CP9. The output of CP9 is connected to AMP9 which is the same as AMP6, and is output as an output voltage Vo9 with a good linearity.

As in Figure 11, the addition portion AD52 includes capacitive coupling CP10 having capacitances C101 and C102 corresponding to AD1p and AD1m connected to them. An output of normalized addition of AD52 is connected to inverted amplifying portion AMP10 similar to AMP6. An output of CP10 is generated in the output of AMP10 with good

linearity. Here it is settled that V101 and V102 are the voltages relative to a basis of the reference voltage Vr, and C101=C102=CF10/2.

As in Figure 12, addition portion AD53 includes a capacitive coupling CP11 having capacitances C111, C112 and C113 corresponding to addition portions AD1p or AD1m and AD52. An output of AD53 is connected to an inverted amplifying portion AMP11 similar to AMP6. An output of normalized addition of CP11 is generated in the output of AMP11 with good linearity. Here it is defined that C111=C112=C113/2=CF11/2. The weight of C113 is settled as the twice of C111 and C112. It is for reducing influence of the normalization in AD52 (to be adjusted to unnormalized V111 and V112). It is prevented that the maximum voltage exceeds the supply voltage by the normalization above.

The reference voltage Vr is generated by a reference voltage generating circuit Vref in Figure 13. The reference voltage generating circuit includes three stages serial inverters I15, I16 and I17, and an output of the last stage is fed back to the first stage input. Similar to the addition portions, unstable oscillation is prevented by a grounded capacitance CG12 and balancing resistances RE121 and RE122. The output of the reference voltage circuit converges to a stable point on which an input and output voltages are equal to each other, and any reference voltage can be generated by changing the threshold of each inverter. Generally, in many cases, it is settled that Vr=Vdd/2 in order to keep dynamic range enough large in both directions of plus and minus. Here, Vdd is the supply voltage of the MOS inverter.

Concerning to the matched filter circuit above, the size of the circuit is largely reduced compared with digital one, and processing speed is high because of parallel multiplication and addition. As the inputs and outputs of the sampling and holding circuit and addition portion are all voltage signals, electric power consumption is low.

In a filter circuit according to the present invention, a matched filter and a sliding correlator are used in parallel, the first acuqisition is executed by a matched filter, a correlating operation is executed by a sliding correlator and a voltage is stopped to supply to the matched filter. Therefore, it is possible to control electric power consumption in minimum and the first acquisition is high speed by the filter circuit according to the present invention.

Claims

1. A filter circuit comprising:

   i) a matched filter connected to an input signal;
   ii) a plurality of sliding correlators parallelly to said matched filter connected to said input signal;
   iii) a timing detecting circuit for detecting timings when an output of said matched filter reach a predetermined or high level as many times as a number equal to or less than that of said sliding correlators;
   iv) a controller for settling a basic timing of a multiplication of each said sliding correlator according to an output of said timing detecting circuit;
   v) a time tracker to which basic timings are given by said controller, said basic timings being finely adjusted of said multiplication of said sliding correlator according to an output of said sliding correlator; and
   vi) a voltage supply switch for stopping an operation of said matched filter after completing timing detection by said timing detecting circuit.

2. A filter circuit as claimed in claim 1, further comprising a second voltage supply switch for stopping operations of said sliding correlator and said time tracker during said operation of said matched filter.

Figure 1

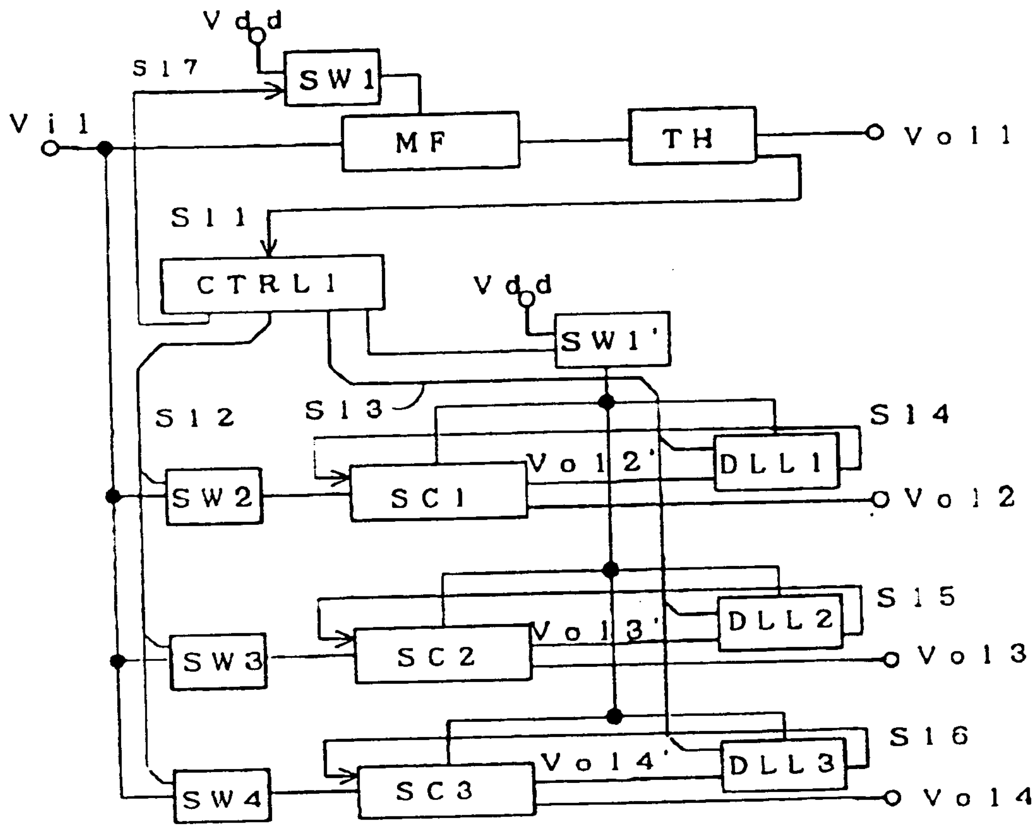


Figure 2

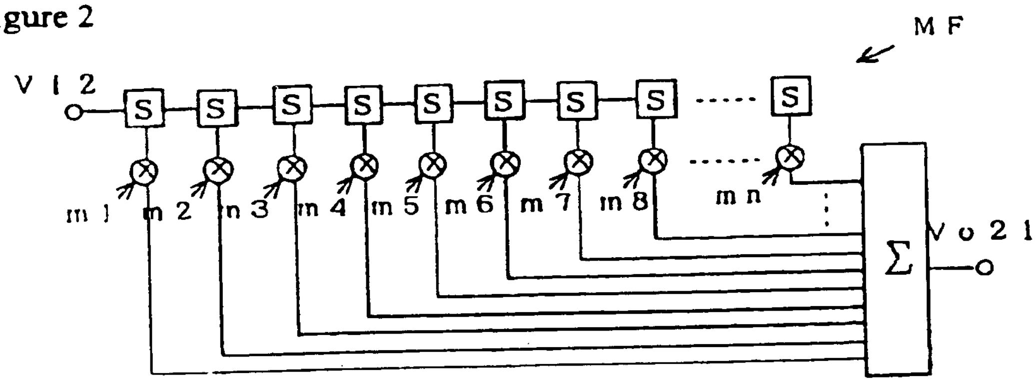


Figure 3

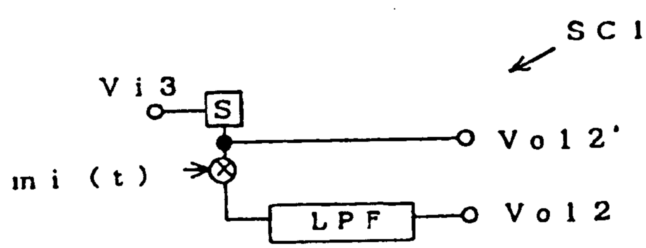


Figure 4

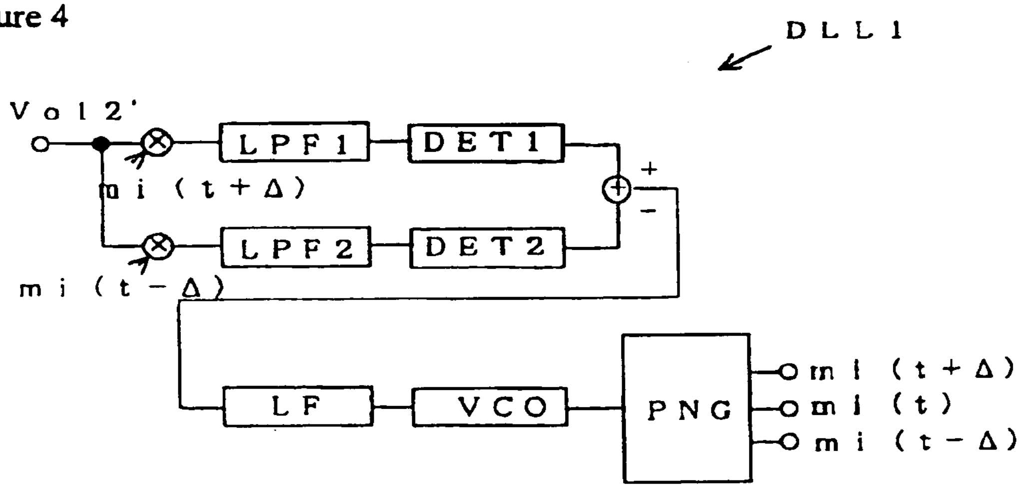


Figure 5

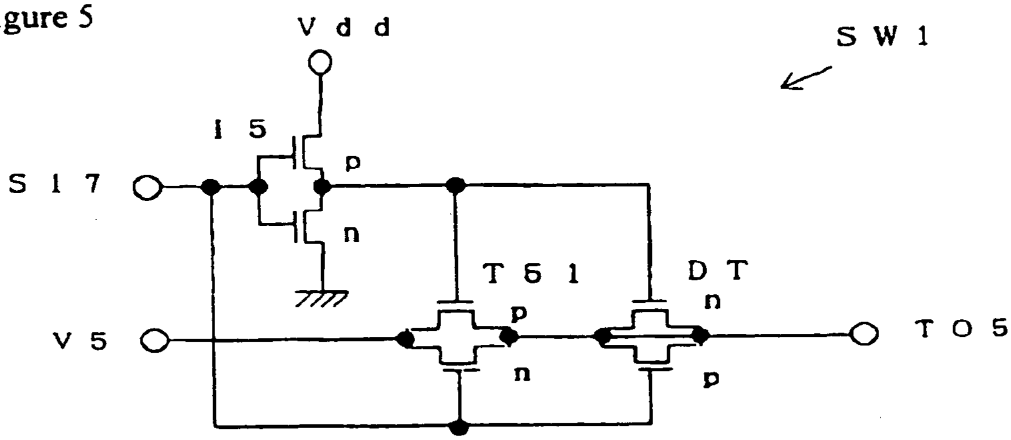


Figure 6

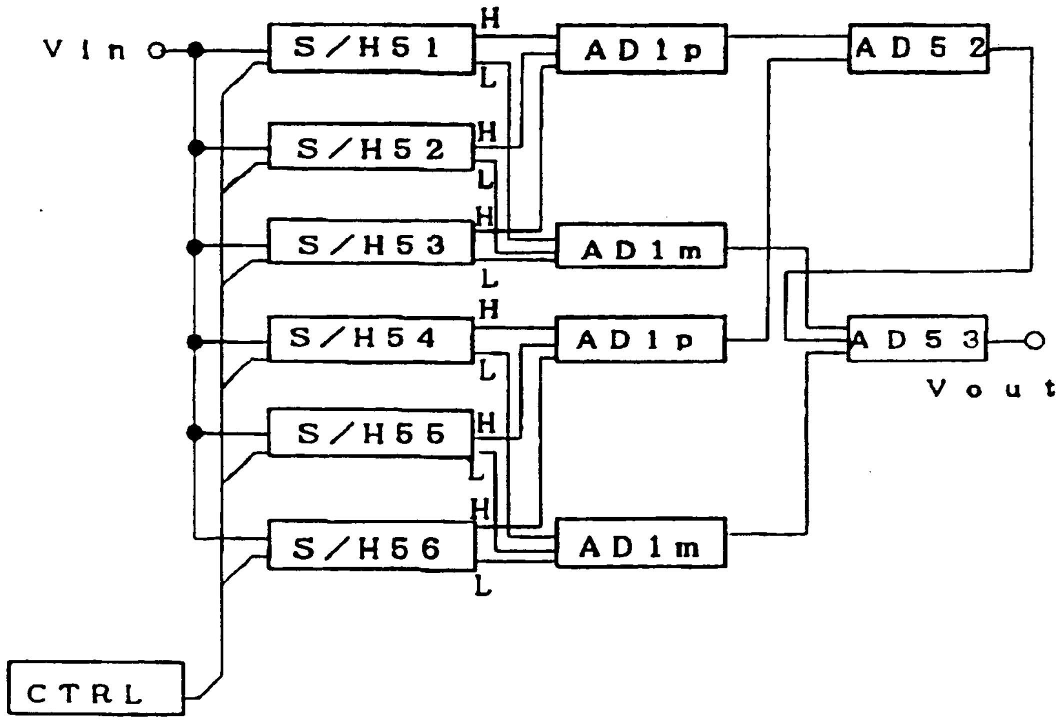
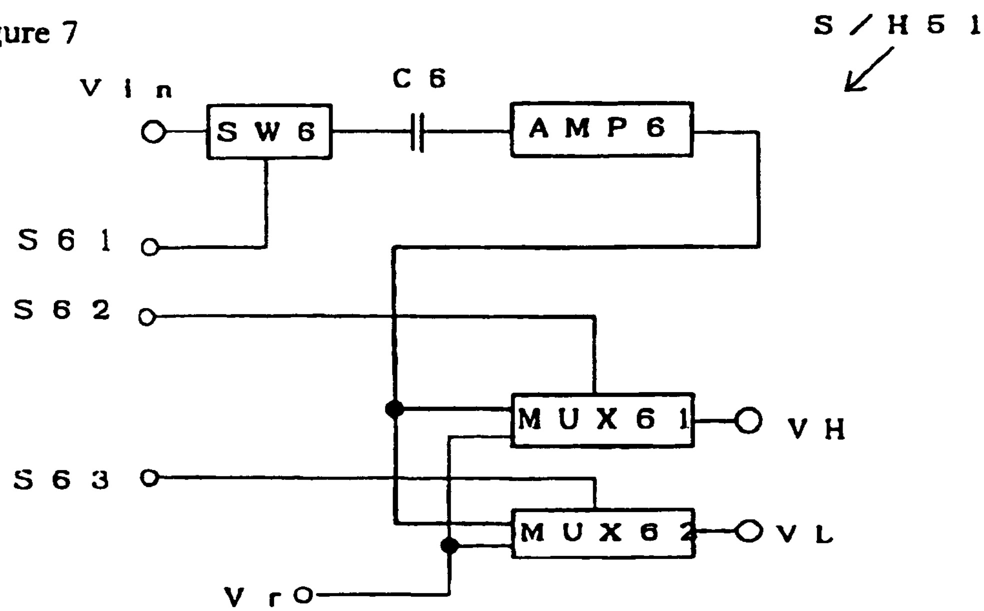


Figure 7



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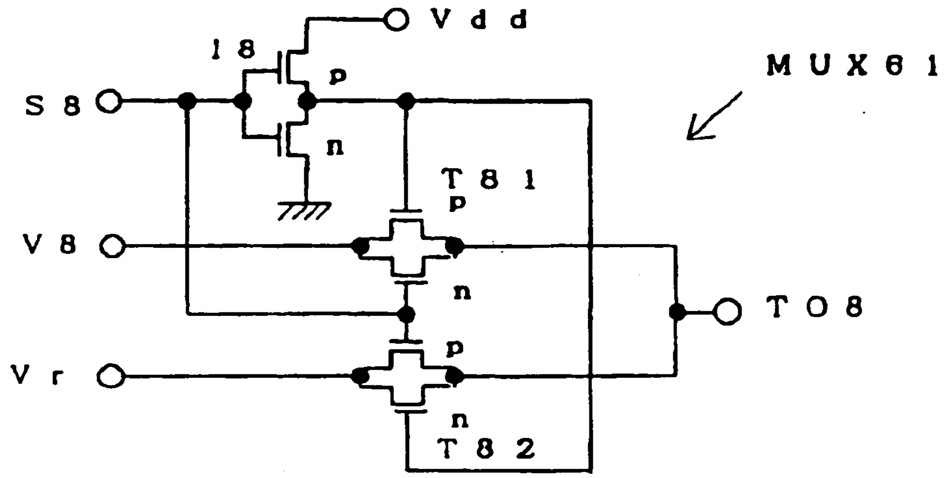


Figure 9

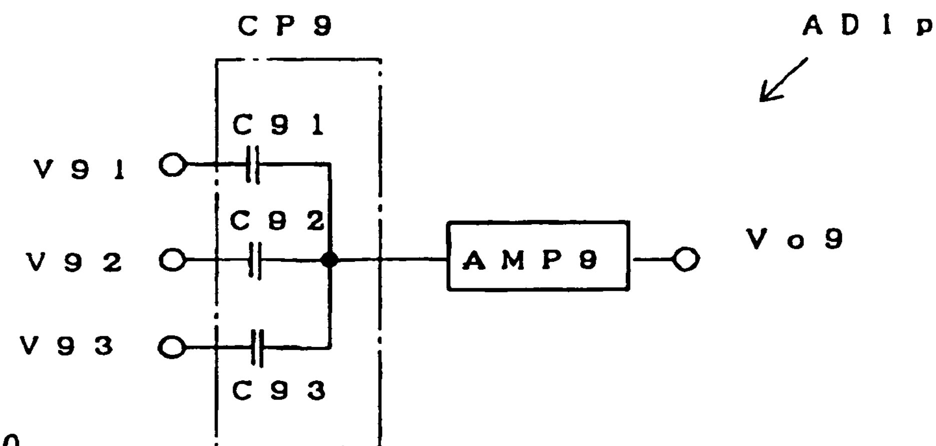


Figure 10

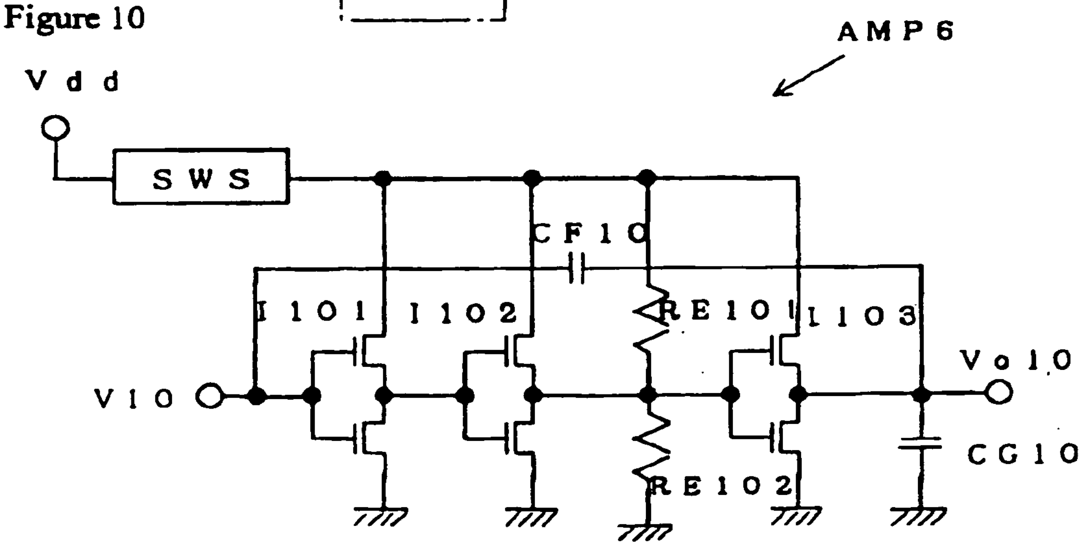


Figure 11

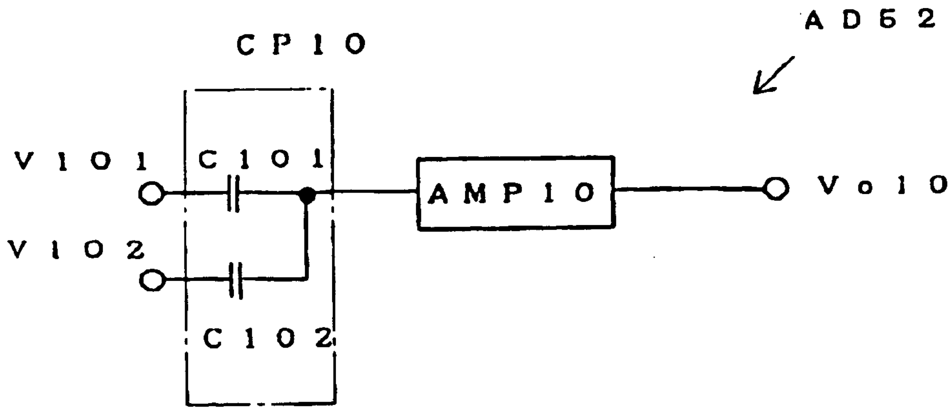
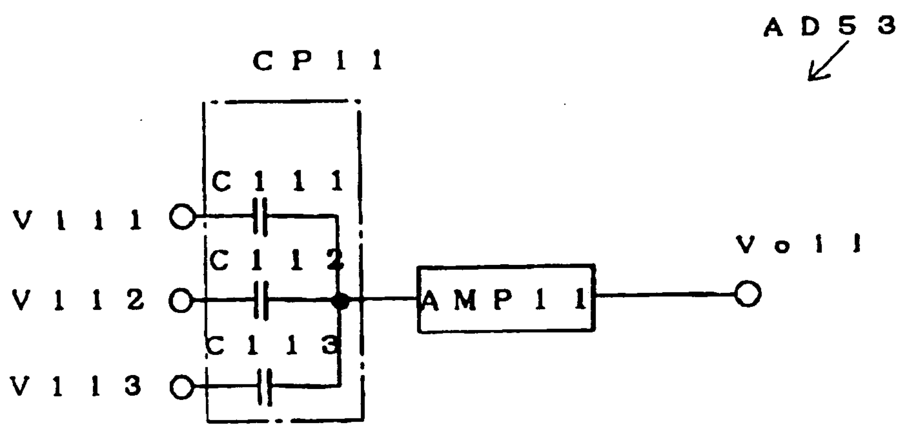


Figure 12



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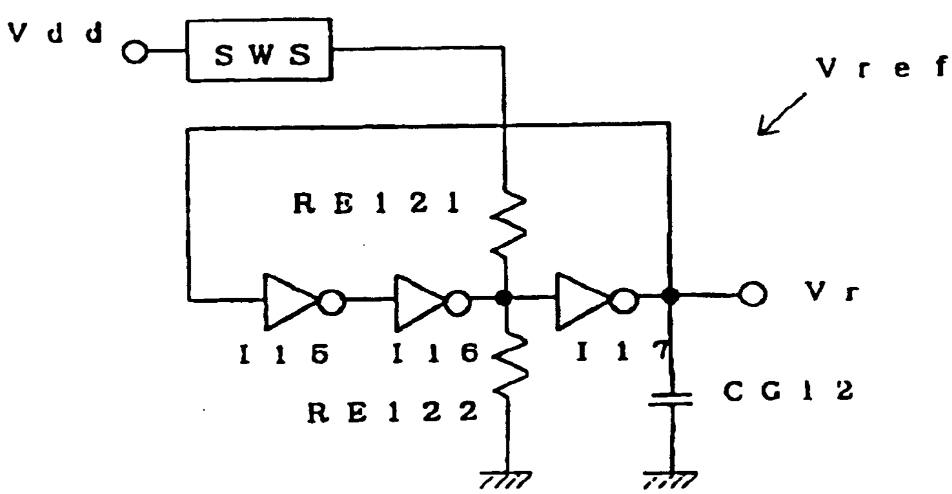
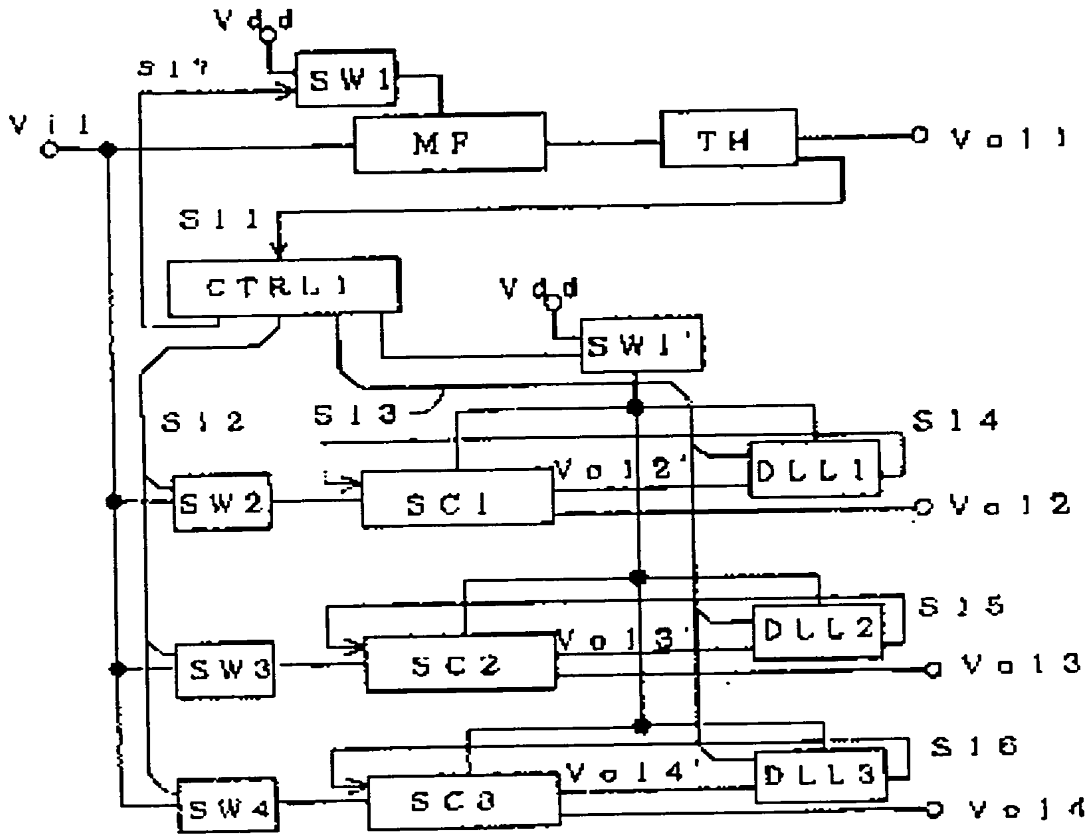


Figure 1



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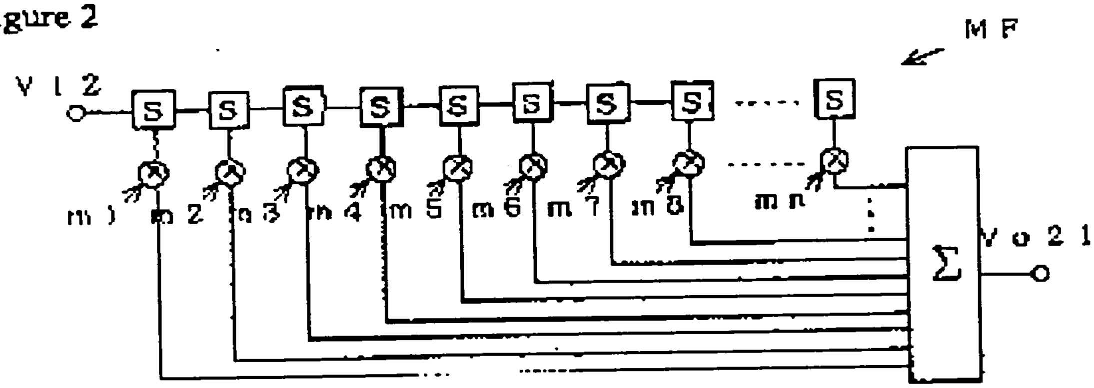

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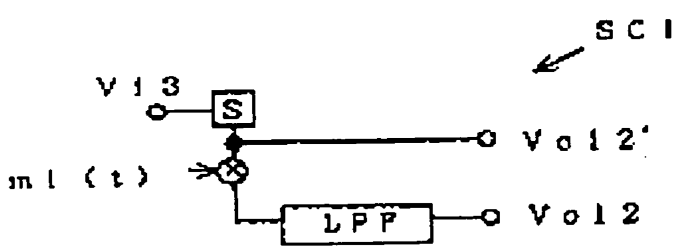

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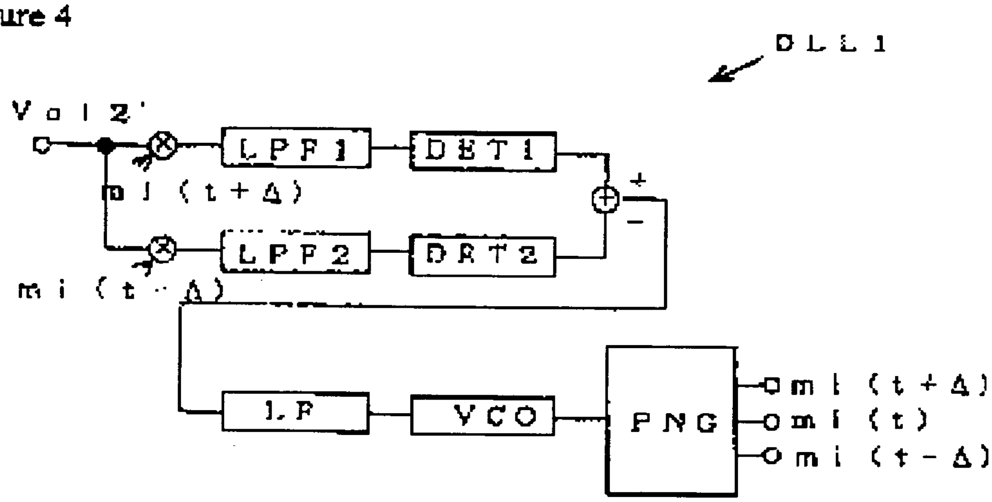

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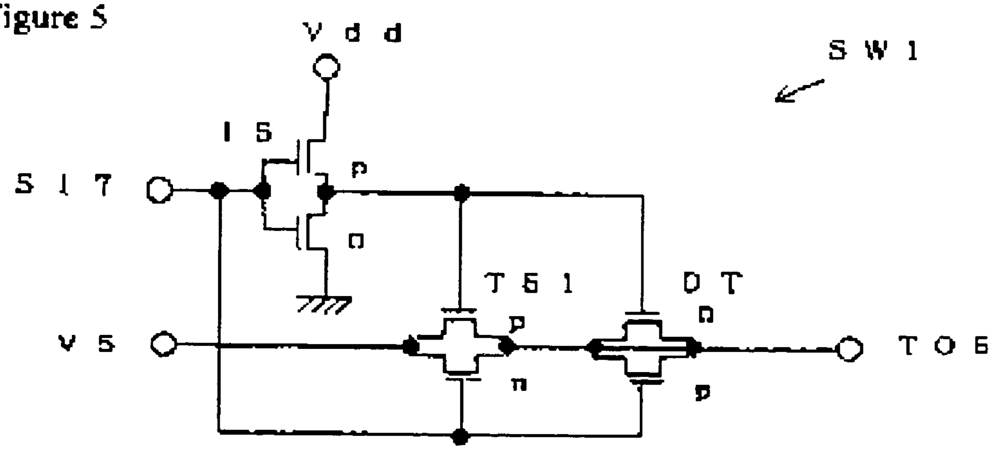
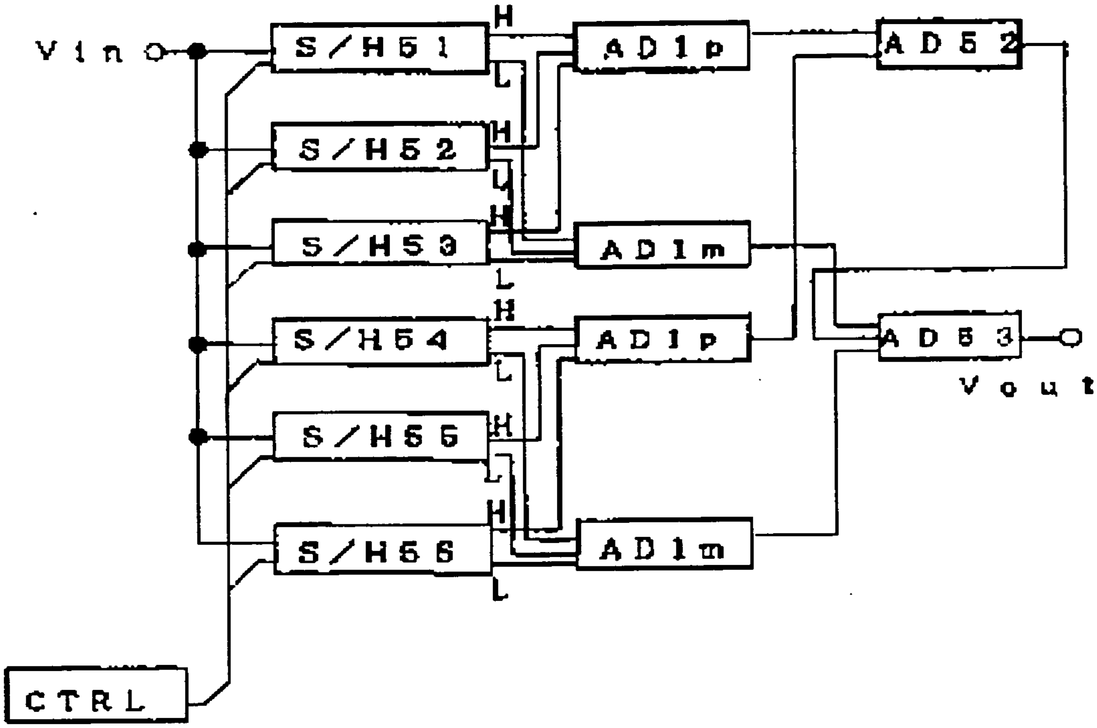


Figure 6



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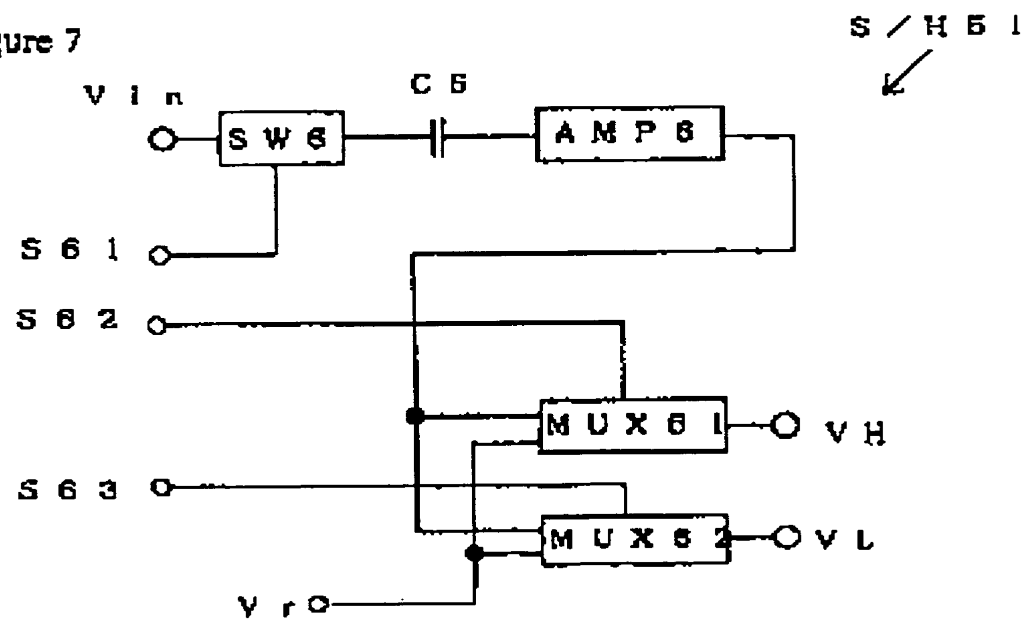
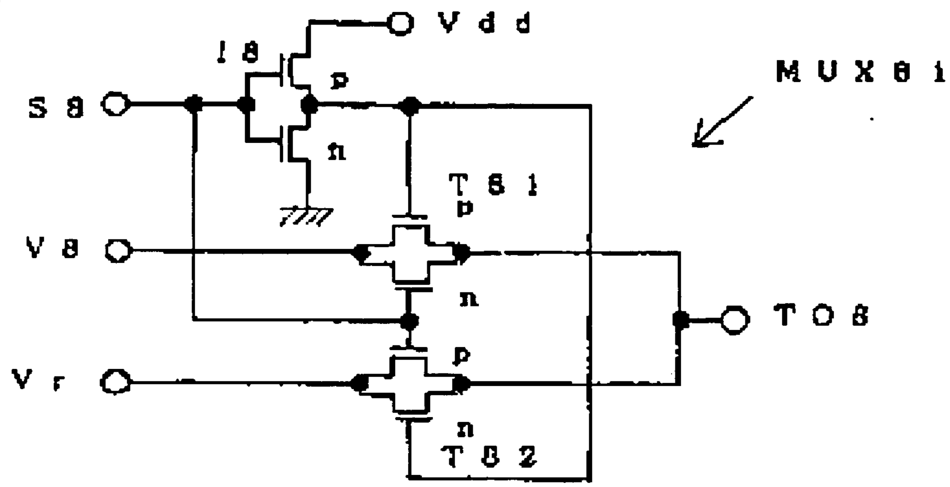


Figure 8



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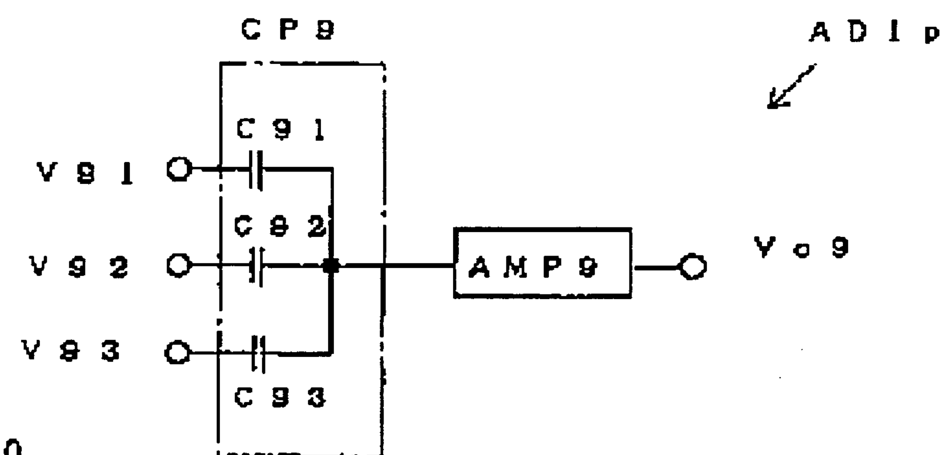

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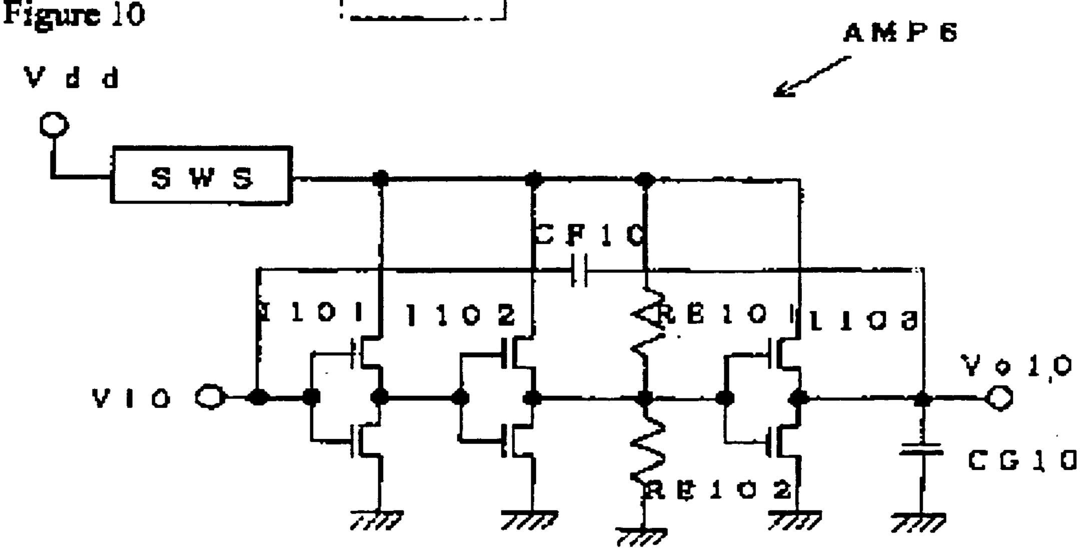


Figure 11

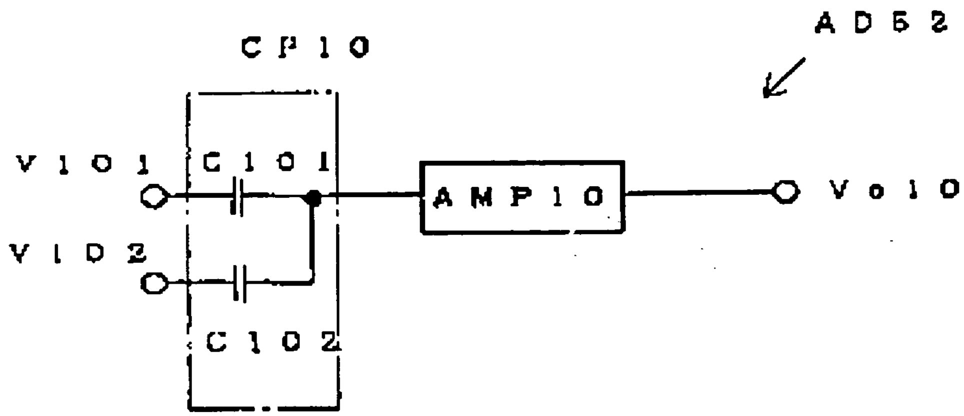


Figure 12

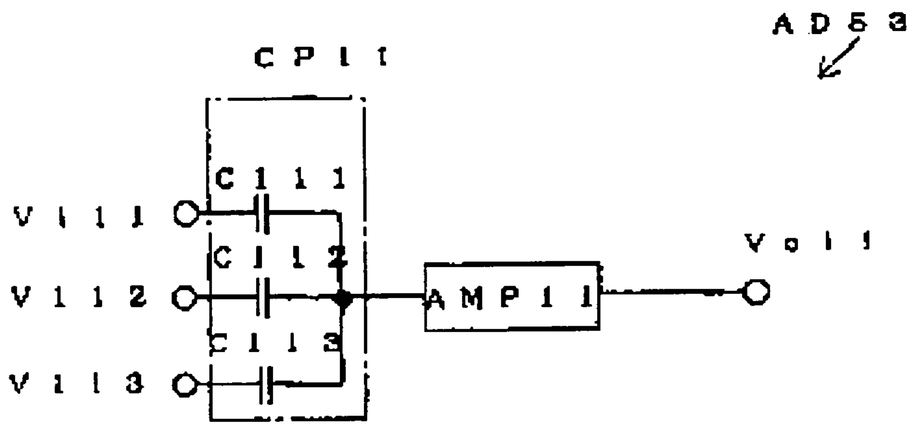
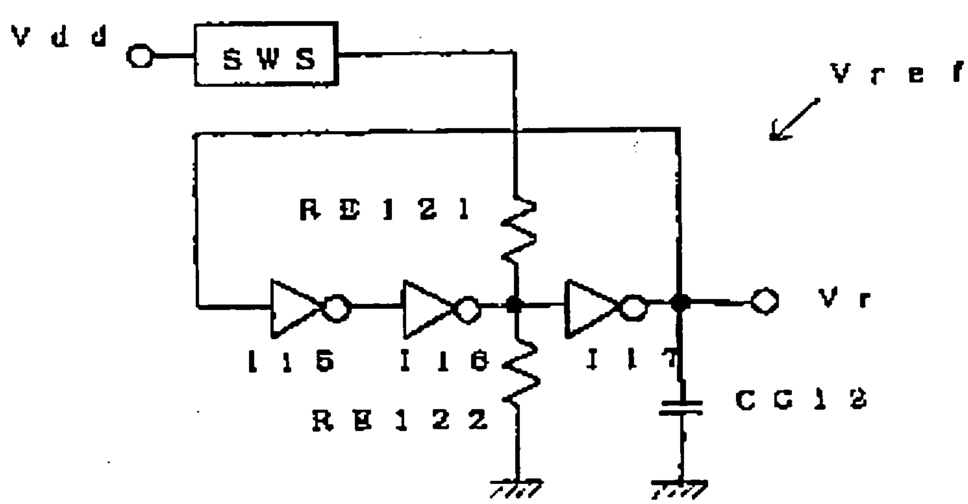


Figure 13



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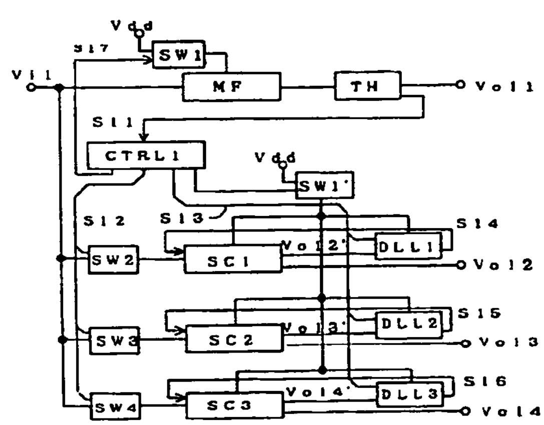
(54) Acquisition and tracking filter for spread spectrum signals

(57) The present invention has an object to provide a filter circuit largely reducing electric power to consume compared with a conventional one, as well as realizing the first acquisition in enough high speed. In a filter circuit according to the present invention, a matched filter and a sliding correlator are used in parallel, the first acquisition and holding is executed by a matched filter, a correlating operation is executed by a sliding correlator and a voltage is stopped to supply to the matched filter.

Figure 1



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EUROPEAN SEARCH REPORT

Application Number
EP 96 11 2313

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	PATENT ABSTRACTS OF JAPAN vol. 018, no. 329 (E-1566), 22 June 1994 (1994-06-22) & JP 06 077932 A (MITSUBISHI ELECTRIC CORP), 18 March 1994 (1994-03-18) * abstract * & US 5 579 338 A (KOJIMA TOSHIHARU) * column 3, line 55 - column 5, line 51 *	1	H04B1/707

TECHNICAL FIELDS SEARCHED (Int.Cl.6)
H04B

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	28 April 2000	Coppieters, S

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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		US 5579338 A	26-11-1996

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82